so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

41. (Amended) The semiconductor device of claim 40 wherein said gate insulating layer comprises silicon dioxide.

48. (Twice Amended) The semiconductor device of claim 40, which comprises a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating; and

wherein said post-fabrication passivation is carried out after formation of at least said gate contact and produces a structure including covalently-bound deuterium populating said interface.

60. (Amended) The semiconductor device of claim 40, wherein said gate insulating layer comprises an oxide of silicon.

61. (Amended) The semiconductor device of claim 40, wherein said gate insulating layer comprises silicon dioxide or silicon oxy nitride.

62. (Amended) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer; said semiconductive device structurally characterized by post-fabrication heating of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C to provide deuterium at and to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

63. (Amended) The semiconductor device of claim 62 wherein said gate insulating layer comprises silicon dioxide.

67 (Amended) The device as recited in claim 66 wherein said film is a dielectric film, and said transistor gate comprises polysilicon .

69 (Amended) The device as recited in claim 68 wherein said transistor gate is comprised of polycrystalline silicon.

72. (Amended) The device as recited in claim 66 wherein said substrate is comprised of a material selected from the group consisting of:
a Group IV element and gallium arsenide.

79 (New). A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, structurally characterized by the gate insulating layer having a thickness not exceeding about 55 Angstroms and by the presence of deuterium at said interface resulting from

post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

80.. (New) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer; said semiconductive device structurally characterized by said gate insulating layer having a thickness not exceeding about 55 Angstroms and by annealing of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature above about 200°C to provide deuterium at said interface between said gate insulating layer and said channel to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

81. (New) An improved semiconductor device including an insulated gate field effect transistor device having a transistor gate and a gate insulator film not exceeding about 55 Angstroms thickness interposed between said transistor and a channel of said transistor device and a concentration of deuterium introduced into and remaining within said film, said transistor device susceptible to degradation associated with hot carrier stress, said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress.